REMARKS

Claim Objections

Claim 14 is concurrently canceled herein, rendering any rejection applied thereto moot. Reconsideration and withdrawal of this rejection are respectfully requested.

Claim Rejections Under 35 USC §112

Claims 7 and 13 are rejected under 35 USC §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Relevant claims have been amended, as needed, to overcome this rejection. Reconsideration and withdrawal of this rejection are respectfully requested.

Claim Rejections Under 35 USC §102

Claims 1-2, 8, and 13-14 are rejected under 35 USC §102(b) as being anticipated by Freeman.

Independent claim 1 is supported by way of an example in Figure 1 and associated written specification, wherein there is indeed disclosed a logic circuit, comprising: a first inversion section 1a for inverting a first input signal **A** having one of positive logic and negative logic and outputting an inverted first input signal **/A**; a second inversion section 1b for inverting a second input signal **XA** having the other of the positive logic and the negative logic and outputting an inverted second input signal **/XA**; and a transmission section 1c for selectively outputting one of the inverted first

input signal /**A** of said first inversion section 1a and the inverted second input signal /**A** of said second inversion section in accordance with a logical value which depends upon an externally controllable selection signal **S** and an inverted signal of the selection signal **XS**.

Therefore, in terms of logical relationship between the first input signal and the second input signal, it is clear that the second input signal is the opposite logic as the first input signal. In other words, if the first input signal is 1, then the second input signal is 0, and vice versa.

To the contrary, as clearly shown in Figure 2 and associated written description of RE34363, while the first input signal is A which is a positive logic, the second input signal is B, which is also a positive logic and not an opposite of the positive logic A. There is no disclosure or teaching in RE34363 that A and B are of opposite logic.

Furthermore, Figure 2 of RE34363 does not disclose or teach an externally controllable selection signal Cs and as inverted signal of the selection signal /Cs as positively asserted in the outstanding final Office action. C2, /C2, C3 and /C3 of RE 34363 should not be confused as an equivalent of S and XS of the present invention, because they do not serve the same functions as explained in the paragraph bridging page 28 line 9 and page 29 line 6 of the written specification in the present invention.

Regarding claim 2, this claim is supported by way of an example in Figure 2, wherein there is indeed disclosed a logic circuit, comprising: a first inversion section 2a for inverting a first input signal A1 and outputting the inverted signal XA1; a second inversion section 2b for inverting a second input signal A2 and outputting the inverted signal XA2; a first outputting section 2c for selectively outputting one of the output XA1 of said first inversion section 2a and the output XA2

of said second inversion section 2b in accordance with a logical value which depends upon an externally controllable first selection signal S1and an inverted signal XS1of the first selection signal S1; and a second outputting section 2d for selectively outputting one of the output XA1 of said first inversion section 2a and the output XA2 of said second inversion section 2b in accordance with a logical value which depends upon an externally controllable second selection signal S2 and an inverted signal XS2 of the second selection signal.

The claim language has specifically recited a first outputting section 2c for selectively outputting one of the output XA1 of said first inversion section 2a and the output XA2 of said second inversion section 2b in accordance with a logical value which depends upon an externally controllable first selection signal S1and an inverted signal XS1of the first selection signal S1; and a second outputting section2d for selectively outputting one of the output XA1 of said first inversion section 2a and the output XA2 of said second inversion section 2b in accordance with a logical value which depends upon an externally controllable second selection signal S2 and an inverted signal XS2 of the second selection signal. These features are simply not disclosed in Figure 2 of RE 34363, as alleged in the outstanding Office action.

In claim 2, the first outputting section and the second outputting section commonly use the first inversion section and the second inversion section (p. 31 line 20 – p. 32 line 3) as double inverter circuits (p. 30 lines 6-8) for obtaining inverted signals, which can reduce a circuit scale. Without a complicated circuit configuration, the present logic circuit can be formed with low loads and in a simple circuit configuration.

Regarding claim 8, this claim is supported by way of an example in Figure 20, wherein there is indeed, further to claim 1, disclosed a first switching section 5a provided on an input side of said first inversion section 1a and capable of performing switching of whether the first input signal XA should be passed or blocked in accordance with an external control signal I or XI; and a second switching section 5b provided on an input side of said second inversion section 1b and capable of performing switching of whether the second input signal A should be passed or blocked in accordance with the external control signal XI or I.

These further features in addition to those in independent claim 1 are simply not disclosed in Figure 2 of RE 34363. The Office interpretation of Figure 2 of Re 34363 is merely a reiteration of what has been stated regarding claim 1. However, the body of claim 8 recite features in addition to what has been recited in claim 1; for example, the first switching section 5a and the second switching section 5b are in addition to what is disclosed in Figure 1 of the present invention. There is simply no equivalent of these sections in Figure 2 of RE 34363.

In claim 8, a high speed operation is obtained, an isolation is strengthened, further, a circuit configuration can be simplified (specification in p. 72 lines 2-11).

Regarding claim 13, relevant portion this claim has specifically stated that "a first inversion section for inverting a first input signal having one of positive logic and negative logic and outputting an inverted first input signal, said first inversion section being essentially composed of transistor circuits, each of said transistor circuits having a first input signal terminal for the first input signal, a first input selection signal terminal for the controllable selection signal and an outputting terminal for outputting the selection signal or the inverted signal based on the logic of

the first input signal."

It is clear from the claim language that there are two transistors for example as shown in Figure 1 of the present application as reference identifiers 1aa and 1ab. Each of transistors 1aa and 1ab has an input terminal for receiving a same first input signal A. These features are not disclosed in Figure 2 of RE 34363, because as clearly shown in Figure 2 of RE34363, transistor 29c receives an input signal A whereas transistor 29d receives an input signal B.

It is well settled that:

> "A claim is anticipated only if each and every element *as set forth in the claim* is found, either expressly or inherently described, in a single prior art reference." *Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1567, 7 USPQ2d 1057 (Fed. Cir. 1988)."

Should the Office continue to believe that the claimed invention is still anticipated by the asserted prior art, a citation of where each and every claimed feature, either as column number and line number, or figure number and reference numeral, or a combination thereof, as disclosed in the asserted prior art is respectfully requested. Should the Office determine that any claimed feature is not disclosed in the asserted prior art, it is respectfully submitted that the claimed invention is not anticipated by the asserted prior art. Allowance of the claimed invention is then respectfully requested.

Allowable Subject Matter

The indication of allowable subject matter in claim 7 is noted with appreciation. Claim 7 has been amended, as needed, to overcome the vague and indefiniteness rejection. Therefore, claim 7 is believed to have been placed in condition for allowance. Allowance of claim 7 is respectfully requested.

CONCLUSION

In view of the aforementioned amendments and accompanying remarks, all pending claims are believed to be in condition for allowance, which action, at an early date, is requested.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 50-2866.

Respectfully Submitted,

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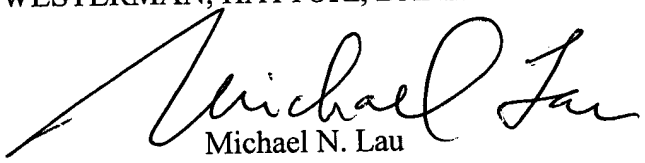

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